

JEDEC STANDARD

Unified Wide Power Supply Voltage Range CMOS DC Interface Standard for Non-Terminated Digital Integrated Circuits

JESD8-23

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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UNIFIED WIDE POWER SUPPLY VOLTAGE RANGE CMOS DC INTERFACE STANDARD FOR NON-TERMINATED DIGITAL INTEGRATED CIRCUITS

(From JEDEC Board Ballot JCB-09-50, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines DC interface parameters and test conditions for a family of non-terminated CMOS digital circuits intended for use over a wide power supply voltage range. The standard bridges a number of existing JEDEC standards in the JESD8-x family to facilitate applications that operate over an ultra-wide power supply voltage range in order to achieve lower power dissipation or higher performance. Three voltage range categories (1, 2 and 3) are defined to support a variety of application requirements. A design claiming compliance with the standard must specifically identify the category or categories supported. This standard specifically does not include interfaces to DDR2 (JESD79-2) or DDR3 (JESD79-3) devices.

2 Standard specification

All voltages are referenced to ground except where noted.

2.1 Absolute maximum continuous ratings

Parameter	Category	Range	NOTE
Supply Voltage, V_{DD}	1	-0.5 V to 4.6 V	1
	2	-0.5 V to 3.6 V	1
	3	-0.5 V to 2.5 V	1
dc Input Voltage, V_{IN} (except I/O pins)		-0.5 V to $V_{DD} + 0.5$ V	1,2,3
dc Output Voltage, V_{OUT} (including I/O pins)		-0.5 V to $V_{DD} + 0.5$ V	2,3
dc Input Diode Current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > V_{DD}$)		+/- 20mA	
dc Output Diode Current, I_{OK} ($V_{OUT} < 0$ or $V_{OUT} > V_{DD}$)		+/- 20mA	

NOTE 1 Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum conditions is not implied.

NOTE 2 Not to exceed maximum V_{DD} .

NOTE 3 Range limited to "-0.4 V to $V_{DD} + 0.4$ V" when V_{DD} is less than 1.1V.

2 Standard specifications (cont'd)

2.2 Recommended operating conditions

Symbol	Parameter	Category (NOTE 1)	Operating Range (NOTE 2)
V_{DD}	Power Supply Voltage	1	1.65 V to 3.6 V
		2	1.4 V to 2.7 V
		3	0.7 V to 1.95 V
T_A	Operating Temperature	-	(NOTE 3)

NOTE 1 Categorized by manufacturer for each application. An application may support one or more categories.

NOTE 2 Specified according to recommended operating conditions for each device.

NOTE 3 Specified by manufacture to be commercial, industrial, and/or military grade.

2.3 DC electrical characteristics

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V_{IH}	Input High Voltage		$0.7V_{DD}$	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage		-0.3	$0.3V_{DD}$	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$	$0.85V_{DD}$	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu A$	-	$0.15V_{DD}$	V

NOTE 1 For V_{IH} and V_{IL} , V_{DD} refers to the receiving device. For V_{OH} and V_{OL} , V_{DD} refers to the sending device.

2.4 DC electrical characteristics for Schmitt trigger operation

Symbol	Parameter	Test Condition	MIN	MAX	Unit
$V_{t+} (V_p)$	Positive Going Threshold Voltage	$V_{OUT} \geq V_{OH} (\min)$	$0.35V_{DD}$	$0.75V_{DD}$	V
$V_{t-} (V_n)$	Negative Going Threshold Voltage	$V_{OUT} \leq V_{OL} (\max)$	$0.25V_{DD}$	$0.65V_{DD}$	V
$V_H (\Delta V_t)$	Hysteresis Voltage	$V_{t+} - V_{t-}$	$0.1V_{DD}$	$0.5V_{DD}$	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$	$0.85V_{DD}$	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu A$	-	$0.15V_{DD}$	V

NOTE 1 For $V_{t+} (V_p)$ and $V_{t-} (V_n)$, V_{DD} refers to the receiving device. For V_{OH} and V_{OL} , V_{DD} refers to the sending device.

3 Test conditions

3.1 Positive Going Threshold Voltage: V_{t+} (V_p)

As the input signal is raised from a ground level in the measurement circuit shown in Figure 1, the input voltage value of which output logic changed is determined as V_{t+} (V_p).

3.2 Negative Going Threshold Voltage: V_{t-} (V_n)

As the input signal is dropped from a power supply voltage level in the measurement circuit shown in Figure 1, the input voltage value of which output logic changed is determined as V_{t-} (V_n).

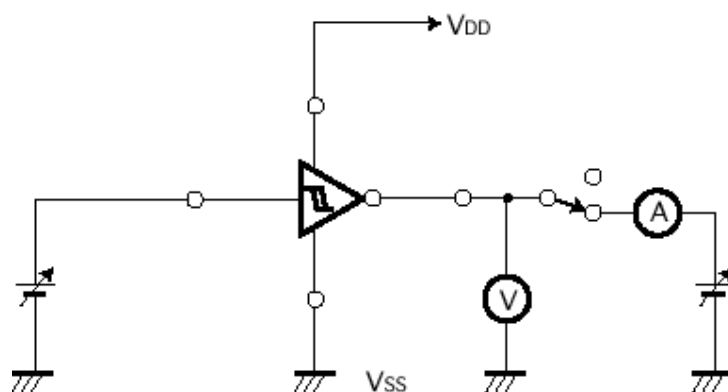


Figure 1 — DC characteristic measurement circuit of Schmitt trigger input



Standard Improvement Form**JEDEC JESD8-23**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

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